Electrical, Electronic and Digital Principles (EEDP)

Lecture 2

BJT Biasing

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Course Info

Title	Electrical, Electronic and Digital Principles (EEDP)
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References	Multiple references will be used
Software Packages	Proteus Design Suite

Course Aims

This unit aims to develop learners' understanding of :

- **The electrical,**
- **Electronic and**
- **Digital principles**

needed for further study of electro-mechanical systems.

Course Contents

1. Apply complex notation in the analysis of single phase circuits

➢ Series and parallel LCR circuits:

- Voltage, current and power with sine wave signals;
- Conditions for resonance

➢ Circuit performance

- Tolerancing (effect of changes in component values)

2. Apply circuit theory to the solution of circuit problems

➢ Circuit theorems:

- Norton - Kirchhoff - Thevenin's
- Superposition - maximum power

➢ Circuit analysis:

- Mesh - nodal
- Impedance matching

Course Contents

3. Understand the operation of electronic amplifier circuits

- Single- and two-stage transistor amplifiers:
  - Class of operation (A, B, AB and C) - analysis of bias - DC conditions
  - AC conditions – coupling- input impedance - output impedance
- Design, test and evaluate a single-stage amplifier to a given specification
  - compare measured (Implemented or simulated) and theoretical results

4. Be able to design and test digital electronic circuits

- Digital electronic devices
- Combinational circuits
- Design and test: circuit designed should be bread-boarded or simulated using an appropriate computer software package

Part 3

3. Understand the operation of electronic amplifier circuits

- ✓ A transistor must be **properly biased** in order to operate as an amplifier.
- ✓ DC biasing is used to establish fixed dc values for the transistor currents and voltages - called the **dc operating point** or **quiescent** point (Q-point).

- ✓ In this lecture, several types of bias circuits are discussed.
- ✓ This part lays the groundwork for the study of amplifiers, and other circuits that require proper biasing.

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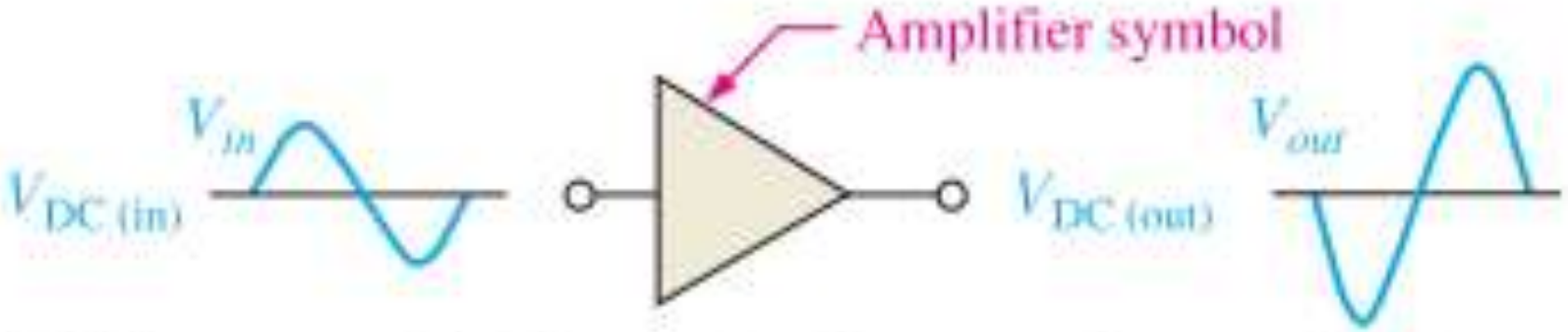
TRANSISTOR BIAS CIRCUITS

- A transistor must be **properly biased** with a dc voltage in order to operate as **a linear amplifier**.
- A dc operating point **must be set** so **that signal variations** at the input terminal are amplified and accurately reproduced at the output terminal.

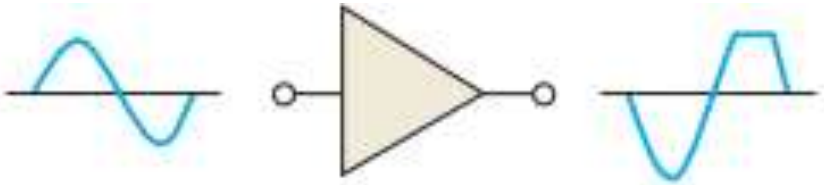


(a) Linear operation: larger output has same shape as input except that it is inverted

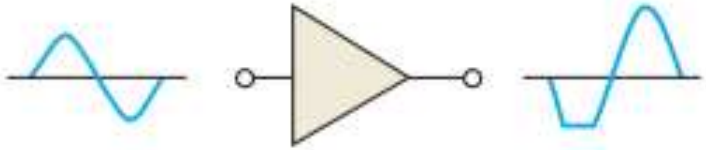
If an amplifier is not biased with correct dc voltages , it can go into **saturation** or **cutoff** when an input signal is applied.

➢ **Improper biasing can cause distortion in the output signal by:**

- ✓ limiting of the **positive portion** of the **output voltage** as a result of a Q-point (dc operating point) being too close to **cutoff**.
- ✓ limiting of the **negative portion** of the **output voltage** as a result of a dc operating point being too close to **saturation**.



(b) Nonlinear operation: output voltage limited (clipped) by cutoff

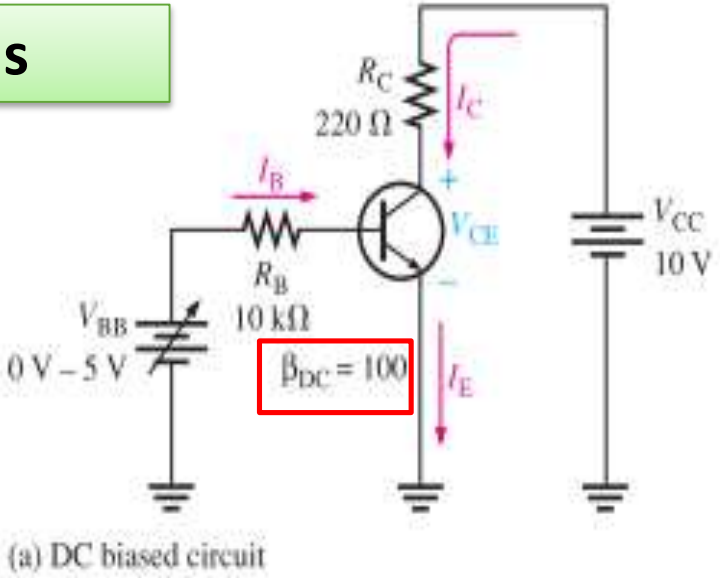


(c) Nonlinear operation: output voltage limited (clipped) by saturation

Graphical Analysis & DC Load Line

❖ Explain graphically the effects of dc bias

- The transistor in Fig. is biased with V_{CC} and V_{BB} to obtain certain values of I_B, I_C, I_E, and V_{CE}.
- V_{BB} is adjusted to obtain different values of I_B



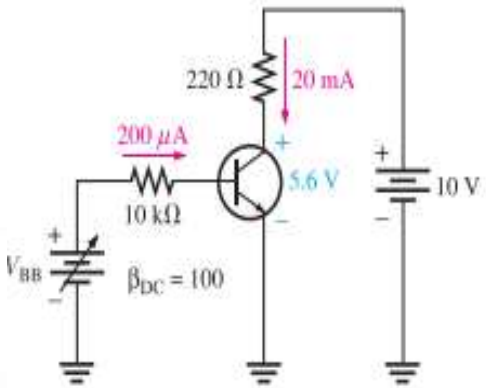
(a) DC biased circuit

First, V_{BB} is adjusted to produce an I_B of 200 μA,

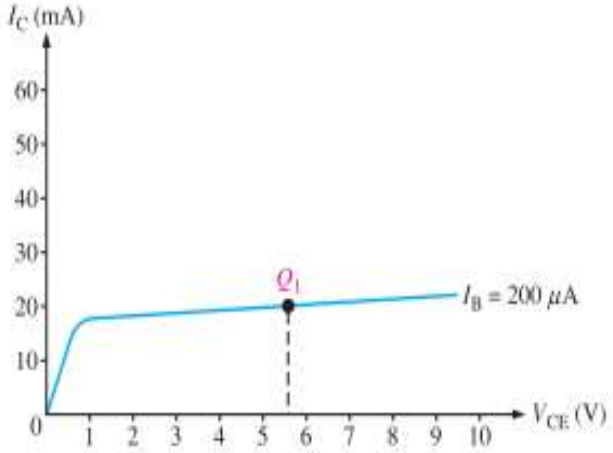
$$I_C = \beta_{DC} I_B = 20\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 10\ \text{V} - (20\ \text{mA})(220\ \Omega) = 10\ \text{V} - 4.4\ \text{V} = 5.6\ \text{V}$$

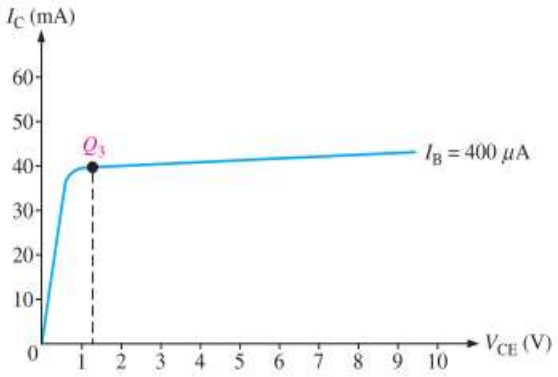
- **Changing VBB will cause changes in all voltages and current (See Next Slide)**

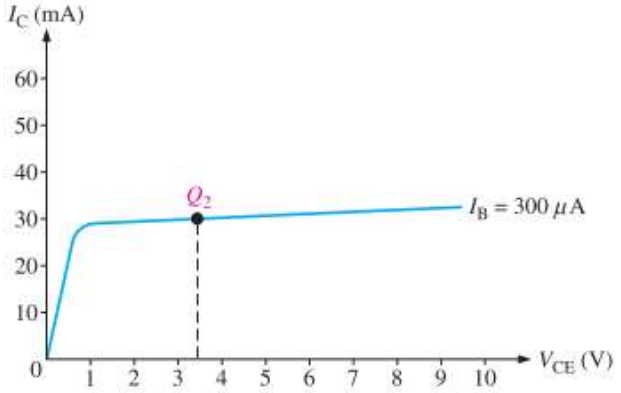


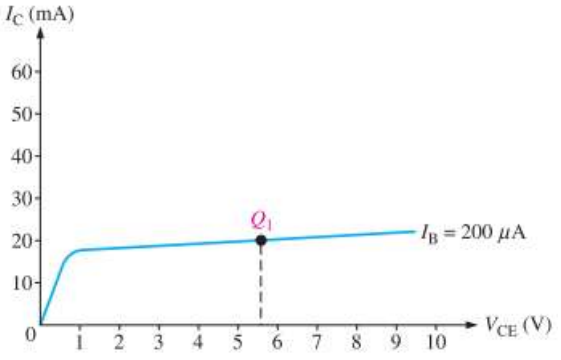
(a) $I_B = 200\ \mu A$



Graphical Analysis & DC Load Line

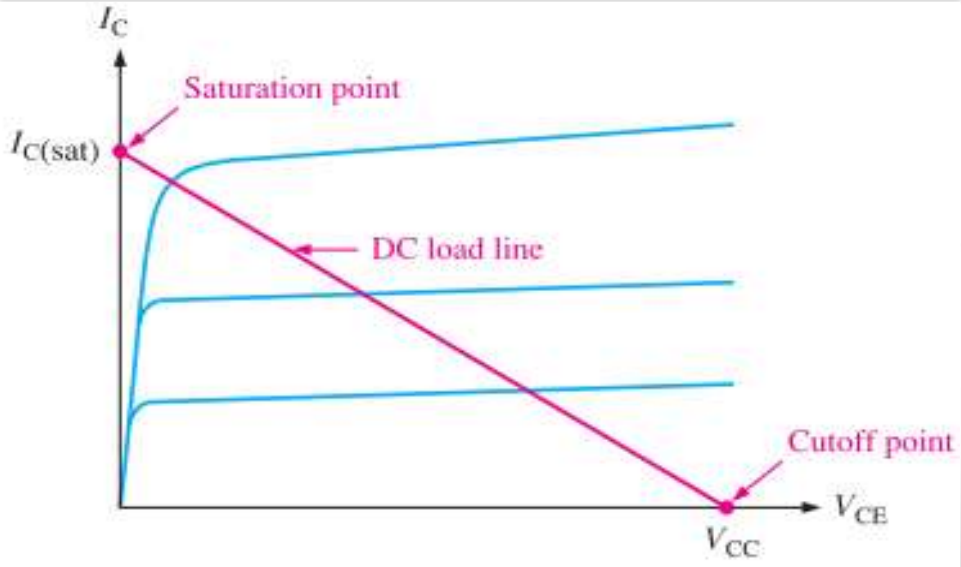


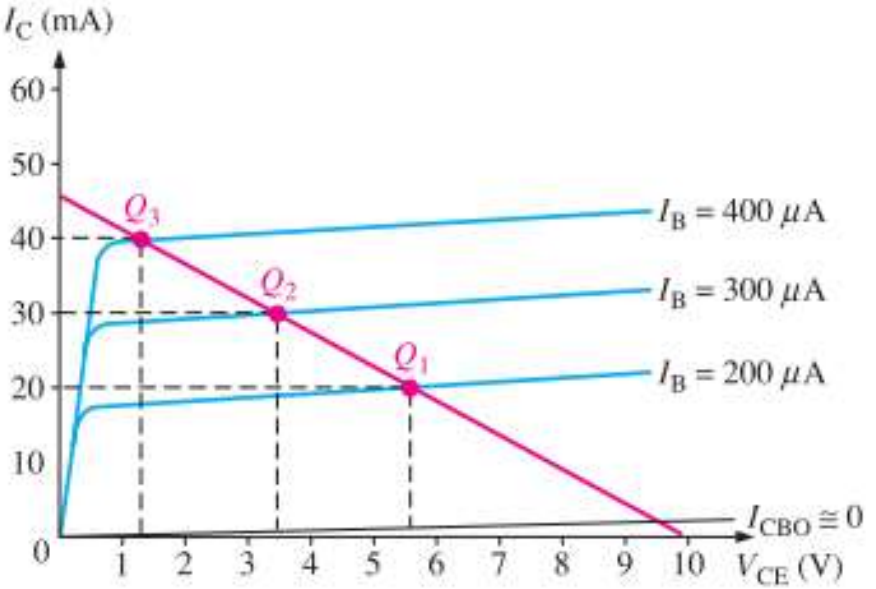




DC Load Line

This is a straight line drawn on the characteristic curves from the saturation value of Ic on the y-axis to the cutoff value of V_{CE} on the x-axis,





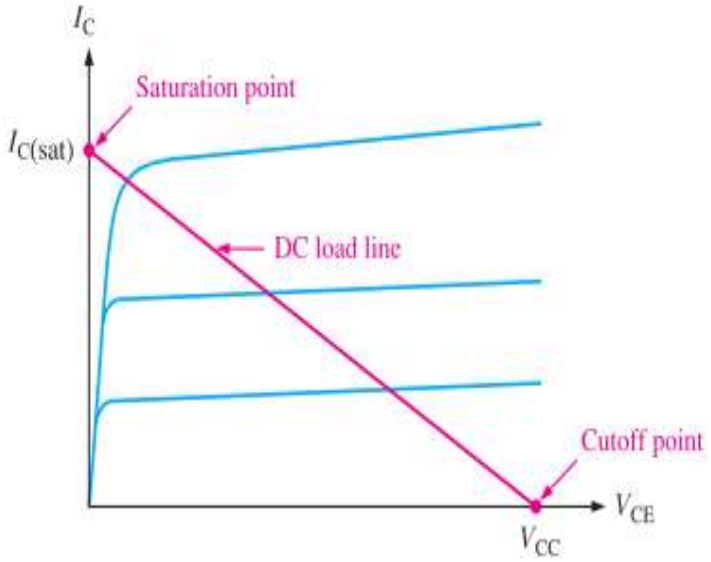
Graphical Analysis & DC Load Line

$$V_{CE} = V_{CC} - I_C R_C$$

When VCE saturates ($V_{CE(sat)}$ near 0):

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

For Ideal Case , let $V_{CE(sat)} = 0$

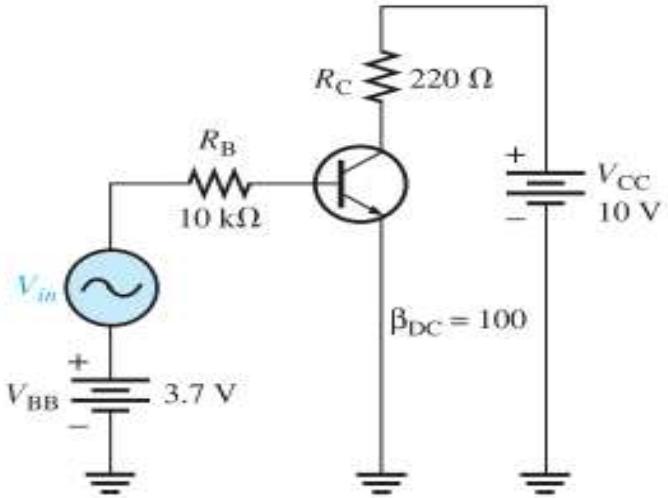


➢ DC Load Line Equation

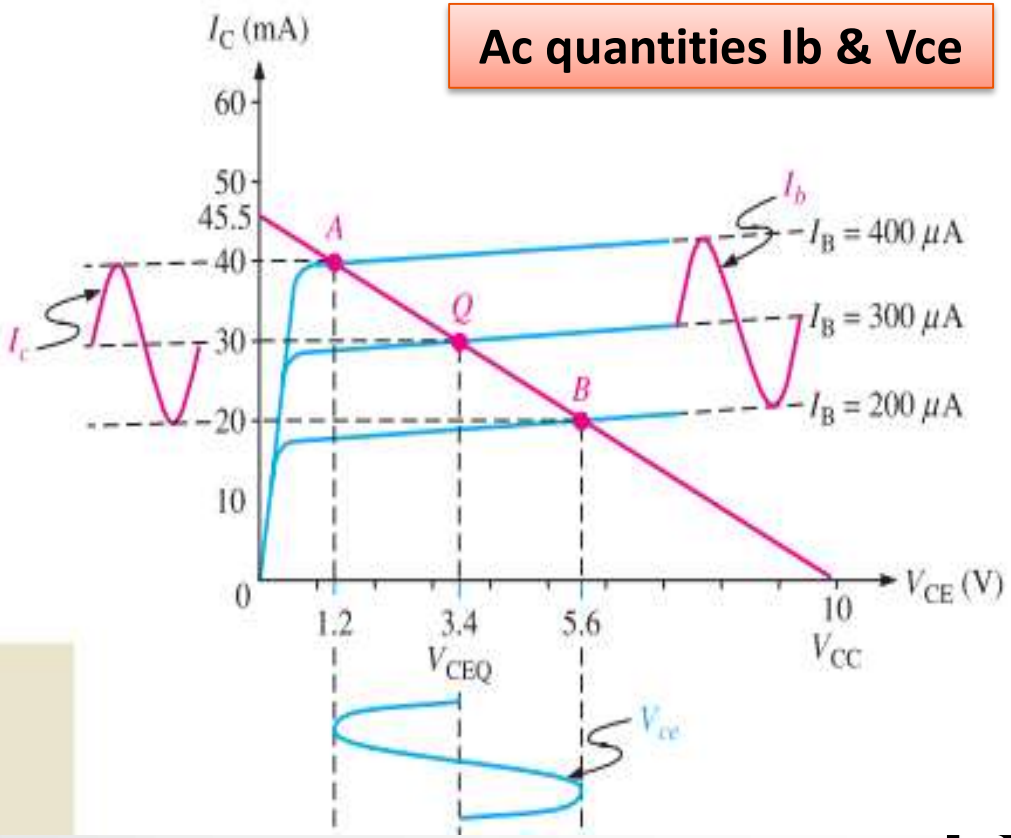
$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} = -\frac{V_{CE}}{R_C} + \frac{V_{CC}}{R_C} = -\left(\frac{1}{R_C}\right)V_{CE} + \frac{V_{CC}}{R_C}$$

Linear Operation

- The region along the load line including all points between saturation and cutoff is generally known as the linear region of the transistor's operation.
- As long as the transistor is operated in this region, the output voltage is ideally a linear reproduction of the input.



Ac quantities Ib & Vce



$$I_{BQ} = \frac{V_{BB} - 0.7\ V}{R_B} = \frac{3.7\ V - 0.7\ V}{10\ k\Omega} = 300\ \mu A$$

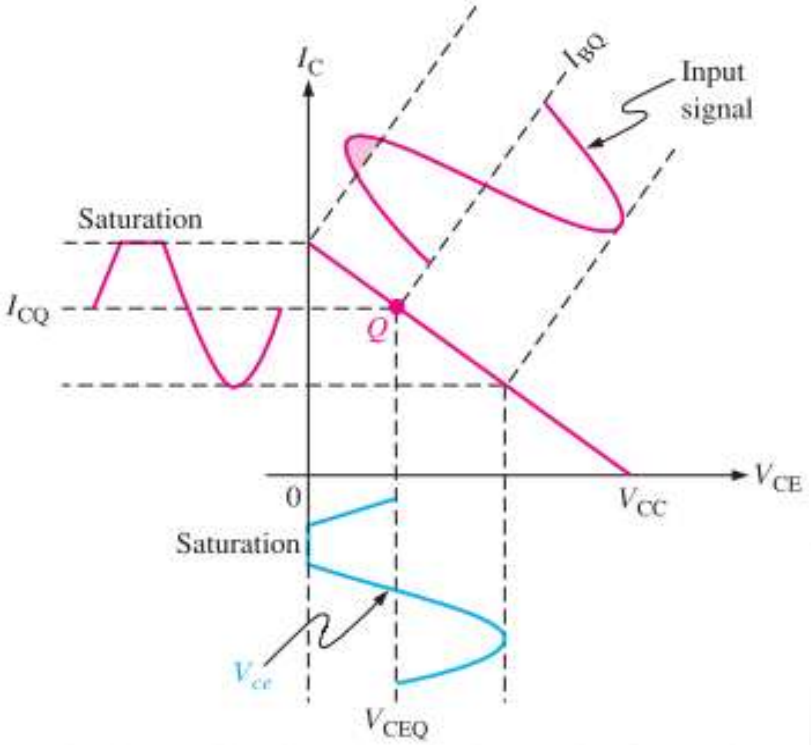
$$I_{CQ} = \beta_{DC} I_{BQ} = (100)(300\ \mu A) = 30\ mA$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10\ V - (30\ mA)(220\ \Omega) = 3.4\ V$$

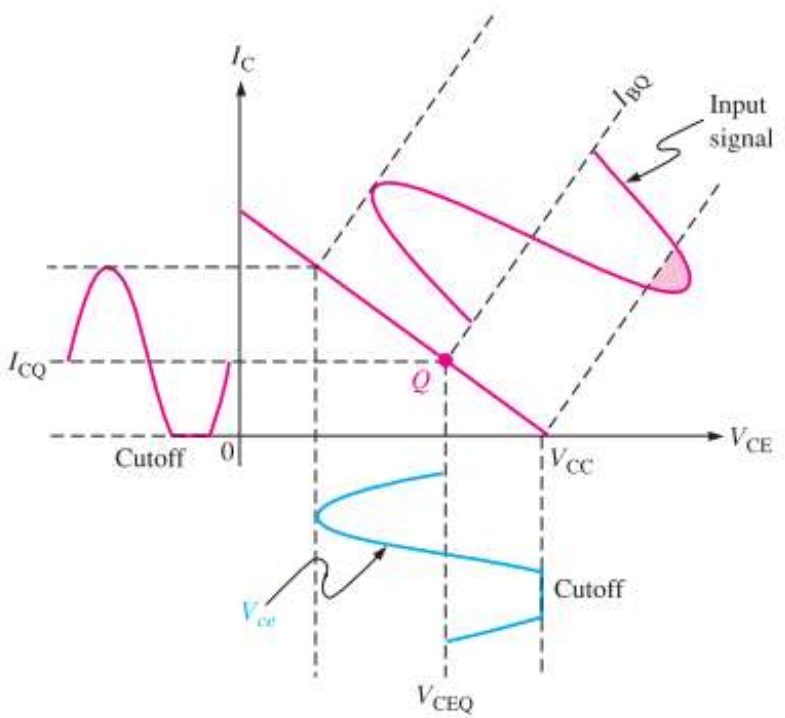
Waveform Distortion

- **Under certain input signal conditions the location of the Q-point on the load line can cause one peak of the Vce waveform to be limited or clipped**

In each case the **input signal** is **too large** for the Q-point location and is driving the transistor into cutoff or saturation during a portion of the input cycle.

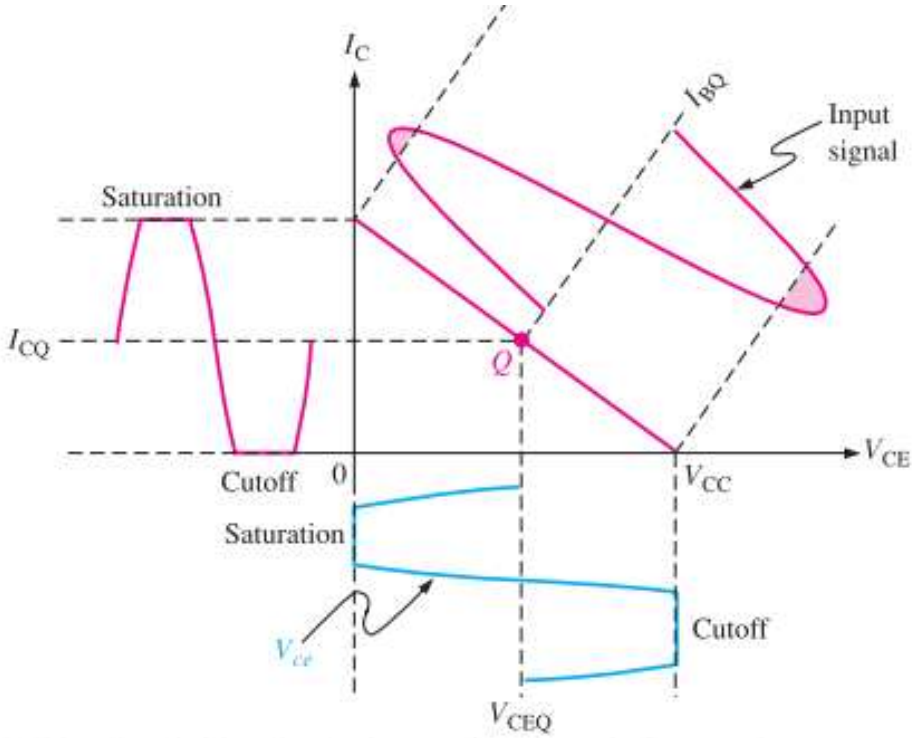


(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.



(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.

Waveform Distortion



(c) Transistor is driven into both saturation and cutoff because the input signal is too large.

Example 5-1

Determine the Q-point for the circuit in Figure 5–7 and draw the dc load line. Find the maximum peak value of base current for linear operation. Assume $\beta_{DC} = 200$.

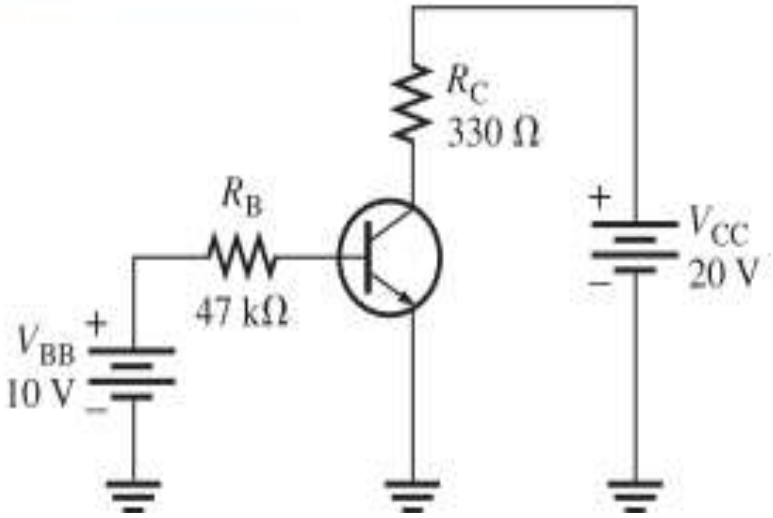
Solution

The Q-point is defined by the values of I_C and V_{CE}.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10\,\text{V} - 0.7\,\text{V}}{47\,\text{k}\Omega} = 198\,\mu\text{A}$$

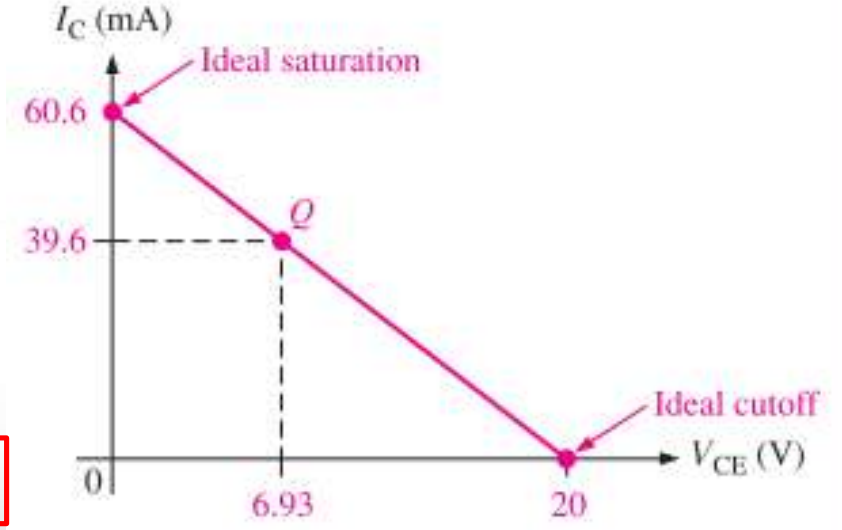
$$I_C = \beta_{DC} I_B = (200)(198\,\mu\text{A}) = \mathbf{39.6\,mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 20\,\text{V} - 13.07\,\text{V} = \mathbf{6.93\,V}$$



$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{20\,\text{V}}{330\,\Omega} = 60.6\,\text{mA}$$

The dc load line is graphically illustrated in Figure



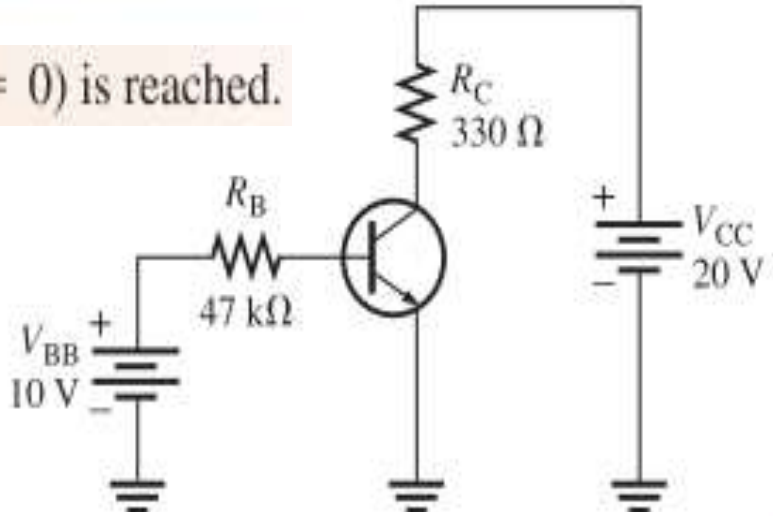
Before saturation is reached, IC can increase an amount ideally equal to:

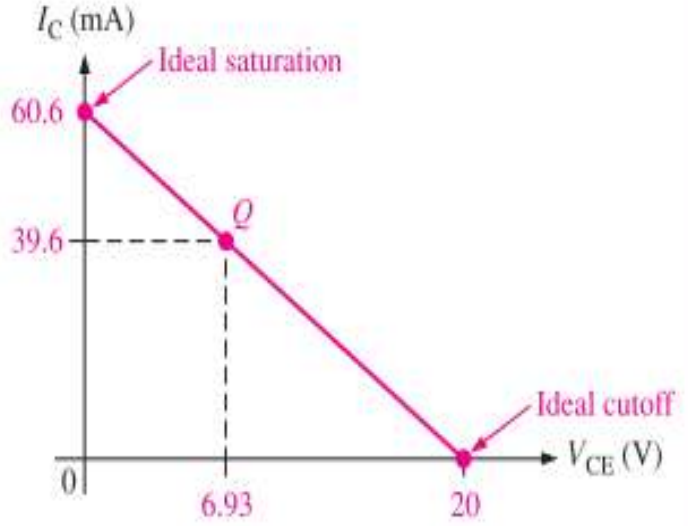
$$I_{C(sat)} - I_{CQ} = 60.6\,\text{mA} - 39.6\,\text{mA} = 21.0\,\text{mA}$$

Example 5-1

However, I_C can decrease by 39.6 mA before cutoff ($I_C = 0$) is reached.

- Therefore, the limiting excursion is 21 mA because the Q-point is closer to saturation than to cutoff
- The 21 mA is the maximum peak variation of the collector current.
- Actually, it would be slightly less in practice because $V_{CE(sat)}$ is not quite zero





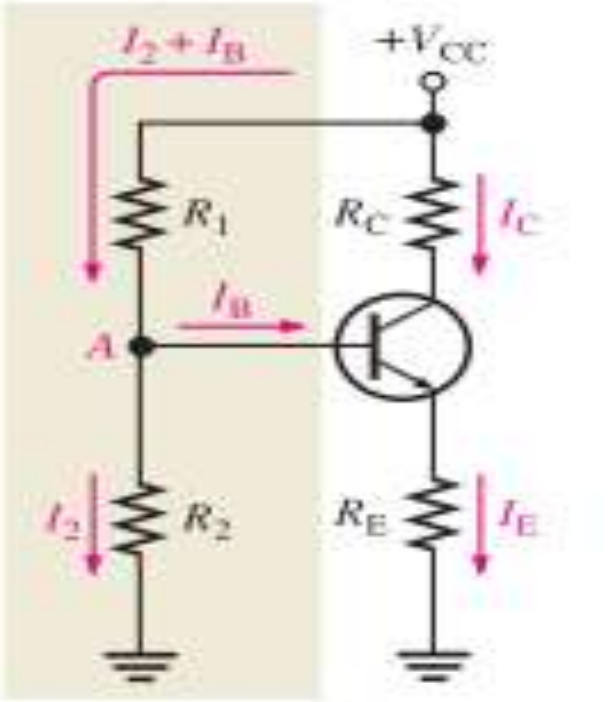
Determine the maximum peak variation of the base current as follows:

$$I_{b(peak)} = \frac{I_{c(peak)}}{\beta_{DC}} = \frac{21\text{ mA}}{200} = \mathbf{105\ \mu A}$$

5–2 VOLTAGE-DIVIDER BIAS

- This is the most widely used biasing method.
- It uses a single-source resistive voltage divider.

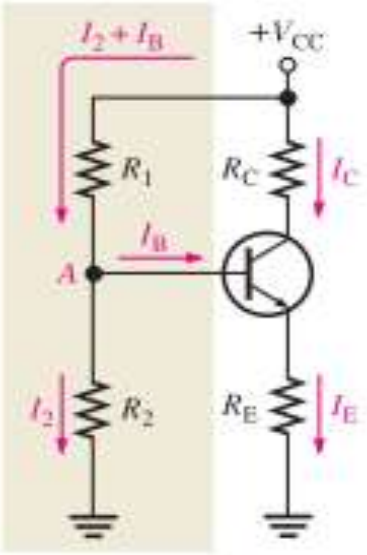
- **To simplify the schematic, the battery symbol is omitted and replaced by a line termination circle with a voltage indicator (Vcc) as shown.**



- Generally, voltage-divider bias circuits are designed so that **the base current** is **much smaller** than the current (I2) through R2
- In this case, the voltage-divider circuit is very straightforward to analyze because **the loading effect** of the base current **can be ignored**.

- ✓ It is called a ((stiff voltage divider)) because the base voltage is relatively **independent** of different transistors and temperature effects.
- ✓ In other words: "**That the transistor does not appear as a significant load**"

Stiff voltage divider circuit analysis



✓ The voltage on the base using the unloaded voltage-divider rule:

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

➢ you can find the voltages and currents in the circuit, as

$$V_E = V_B - V_{BE}$$

$$I_C \cong I_E = \frac{V_E}{R_E}$$

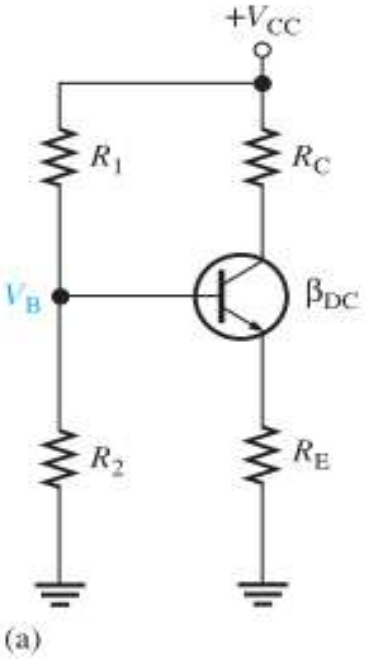
$$V_C = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

Not Completely accurate

Thevenin's Theorem Applied to Voltage-Divider Bias

To analyze a voltage-divider biased transistor circuit for base current loading effects

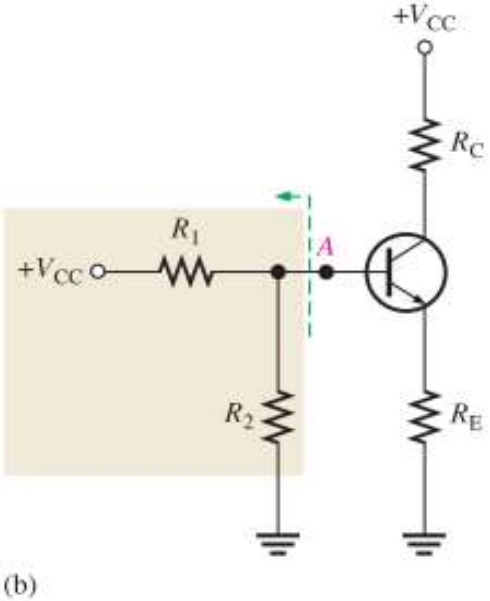


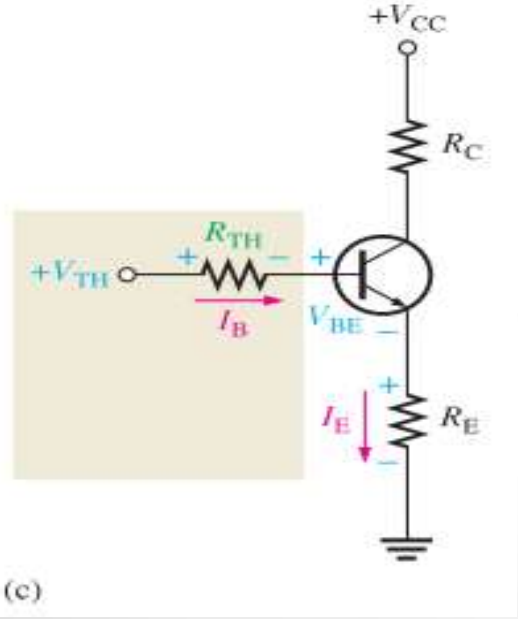
1. let's get an equivalent base-emitter circuit for the circuit in Figure 5–13(a)

2. Apply Thevenin's theorem to the circuit left of point A,

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$





The Thevenin equivalent of the bias circuit, connected to the transistor base

Thevenin's Theorem Applied to Voltage-Divider Bias

3. Applying Kirchhoff's voltage law around the equivalent base-emitter loop gives

$$V_{TH} - V_{R_{TH}} - V_{BE} - V_{R_E} = 0$$

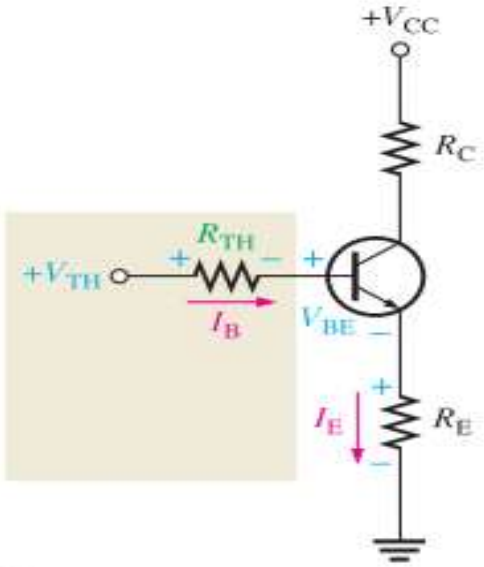
$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

Substituting I_E/β_{DC} for I_B,

$$V_{TH} = I_E(R_E + R_{TH}/\beta_{DC}) + V_{BE}$$

Then solving for I_E,

$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}$$



(c)

If R_{TH}/β_{DC} is small compared to R_E, the result is the same as for an unloaded voltage divider.

➢ If we do not use the current approximation ($I_E = I_C$)

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

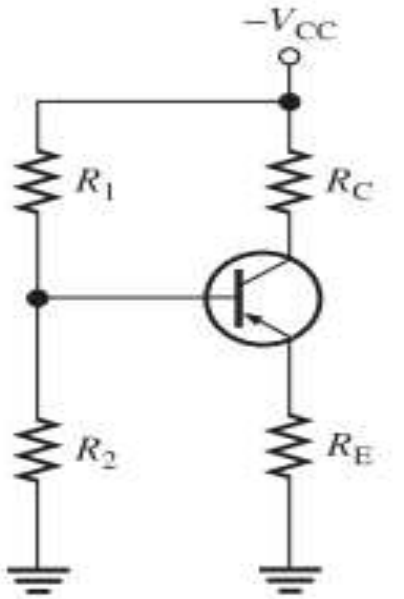
Voltage-Divider Biased PNP Transistor

1. Negative collector supply voltage, Vcc

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

$$I_B = \frac{I_E}{\beta_{DC}}$$



(a) Negative collector supply voltage, V_{CC}

applying Kirchhoff's voltage law

$$V_{TH} + I_B R_{TH} - V_{BE} + I_E R_E = 0$$

$$I_E = \frac{-V_{TH} + V_{BE}}{R_E + R_{TH}/\beta_{DC}}$$

Check EXAMPLE 5–5

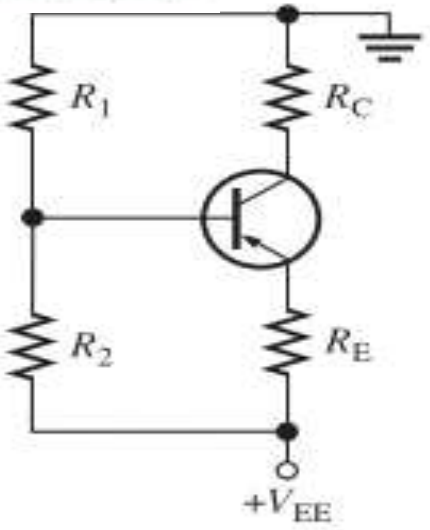
Voltage-Divider Biased PNP Transistor

2. Positive emitter supply voltage, V_{EE}

$$V_{TH} = \left(\frac{R_1}{R_1 + R_2}\right)V_{EE}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

$$I_B = \frac{I_E}{\beta_{DC}}$$

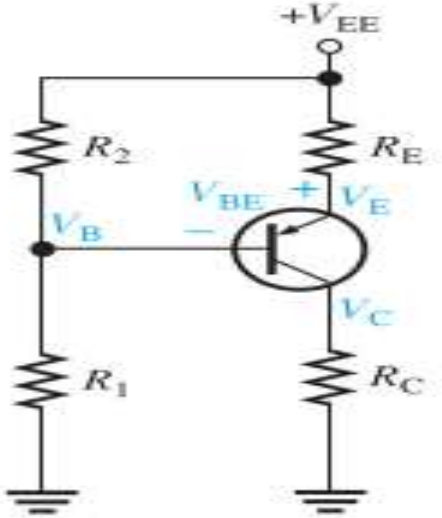


(b) Positive emitter supply voltage, V_{EE}

applying Kirchhoff's voltage law

$$-V_{TH} + I_B R_{TH} - V_{BE} + I_E R_E - V_{EE} = 0$$

$$I_E = \frac{V_{TH} + V_{BE} - V_{EE}}{R_E + R_{TH}/\beta_{DC}}$$



(c) The circuit in (b) redrawn

Check EXAMPLE 5–4